Amendments to the Claims

1. (CURRENTLY AMENDED) Apparatus for processing a differential input signal, the apparatus comprising

-a peak detector ~~(31; 51)~~ with a differential input ~~(28)~~, the peak detector ~~(31; 51)~~ providing a first voltage ~~(42)~~ being proportional to an average voltage peak at the peak detector's differential input ~~(28)~~,

-a compressor ~~(33; 53)~~ processing the first voltage ~~(42)~~ in order to provide a second voltage ~~(42.1)~~,

-a voltage controllable current source ~~(35)~~ providing a trim current ~~(IT)~~ being adjustable by the second voltage ~~(42.1)~~,

-a hysteresis equipped circuit ~~(36; 62.1 - 62.n; 67.1)~~ whose hysteresis characteristics are adjustable by the trim current ~~(IT)~~,

-wherein the peak detector ~~(31; 51)~~ is operationally coupled to the compressor ~~(33; 53)~~ and the compressor ~~(33; 53)~~ is operationally coupled to the voltage controllable current source ~~(35)~~.

2. (CURRENTLY AMENDED) The apparatus of claim 1, wherein the peak detector ~~(31; 51)~~ comprises an integrator.

3. (CURRENTLY AMENDED) The apparatus of claim 1, wherein the peak detector ~~(31; 51)~~ operates on the envelop of a differential input signal ~~(IN1)~~ being applied to the differential input ~~(28)~~.

4. (CURRENTLYA MENDED) The apparatus of ~~claim 1 or 2~~claim 1, wherein the peak detector ~~(31; 51)~~ is designed to constantly follow the average voltage peak at the peak detector's differential input ~~(28)~~.

5. (CURRENTLY AMENDED) The apparatus of ~~claim 1 or 2~~claim 1, providing a hysteresis characteristics depending on the average voltage peak at the peak detector's differential input ~~(28)~~.

6. (CURRENTLY AMENDED) The apparatus of ~~claim 1 or 2~~claim 1, wherein the peak detector ~~(31; 51)~~ comprises a differential input transistor pair at its differential input.

7. (CURRENTLY AMENDED) The apparatus of claim 6, wherein the load conditions of the differential input transistor pair changes when the average voltage peak changes.

8. (CURRENTLY AMENDED) The apparatus of ~~claims 1 or 2~~claim 1, wherein the hysteresis characteristics are adjusted by shifting trip-levels ~~(VT1, VT2)~~ of the hysteresis equipped circuit ~~(36; 62.1 - 62.n; 67.1)~~ to lower levels if the differential input signal is a low level signal and to higher levels if the differential input signal is a high level signal.

9. (CURRENTLY AMENDED) The apparatus of ~~claims 1 or 2~~claim 1, wherein a differential clock signal ~~(CLK+, CLK-)~~ is used as the differential input signal to perform a sensing phase and an appropriate adjustment of the hysteresis characteristics.

10. (CURRENTLY AMENDED) The apparatus of ~~claims 1 or 2~~claim 1, wherein the compressor ~~(33; 53)~~ applies a function ~~(29, g)~~ when processing the first voltage (42) in order to provide the second voltage ~~(42.1)~~.

11. (CURRENTLY AMENDED) Control circuitry ~~(60)~~ for a display system comprising an array of interfaces ~~(61)~~, whereby at least one interface ~~(61.1)~~ comprises

- a peak detector ~~(51)~~ with a differential input ~~(28)~~, the peak detector ~~(51)~~ providing a first voltage being proportional to an average voltage peak of a differential clock signal ~~(CLK+, CLK-)~~ being applied to the peak detector's differential input,
- a compressor ~~(53)~~ processing the first voltage in order to provide a second voltage,
- a voltage controllable current source providing a current ~~(Ifb)~~ being adjustable by the second voltage,

- a hysteresis equipped circuit ~~(62.1 – 62.n; 67.1)~~ whose hysteresis characteristics are adjustable by the current ~~(Ifb)~~.

12. (CURRENTLY AMENDED) The control circuitry ~~(60)~~ of claim 11, wherein a signal ~~(Ifb)~~ is provided by the at least one interface (62.1) to other interfaces ~~(62.2 – 62.n)~~ of the array of interfaces ~~(61)~~ in order to allow the hysteresis characteristics of the other interfaces ~~(62.2 – 62.n)~~ to be adjusted, too.

13. (CURRENTLY AMENDED) The control circuitry ~~(60)~~ of ~~claim 11 or 12~~claim 11, wherein the interfaces ~~(62.1 – 62.n)~~ of the array of interfaces ~~(61)~~ serve as differential RSDS interfaces.

14. (CURRENTLY AMENDED) The control circuitry ~~(60)~~ of ~~claim 11 or 12~~claim 11, wherein the interfaces ~~(62.1 – 62.n)~~ of the array of interfaces ~~(61)~~ serve as low EMI / low power interfaces between timing controllers and digital-to-analog latches employed for driving analog signals onto column electrodes of a display panel of the display system.

15. (CURRENTLY AMENDED) The control circuitry ~~(60)~~ of ~~claim 11 or 12~~ claim 11 further comprising a transmitting circuit for transmitting video data to the array of interfaces ~~(61)~~.

16. (CURRENTLY AMENDED) The control circuitry ~~(60)~~ of claim 15, wherein the array of interfaces ~~(61)~~ converts the video data into analog signals for driving onto column electrodes of a display panel of the display system.

17. (CURRENTLY AMENDED) The control circuitry ~~(60)~~ of ~~claim 14 or 15~~claim 14, wherein any kind of reduced swing signaling can be used to transmit the video data to the array of interfaces ~~(61)~~.